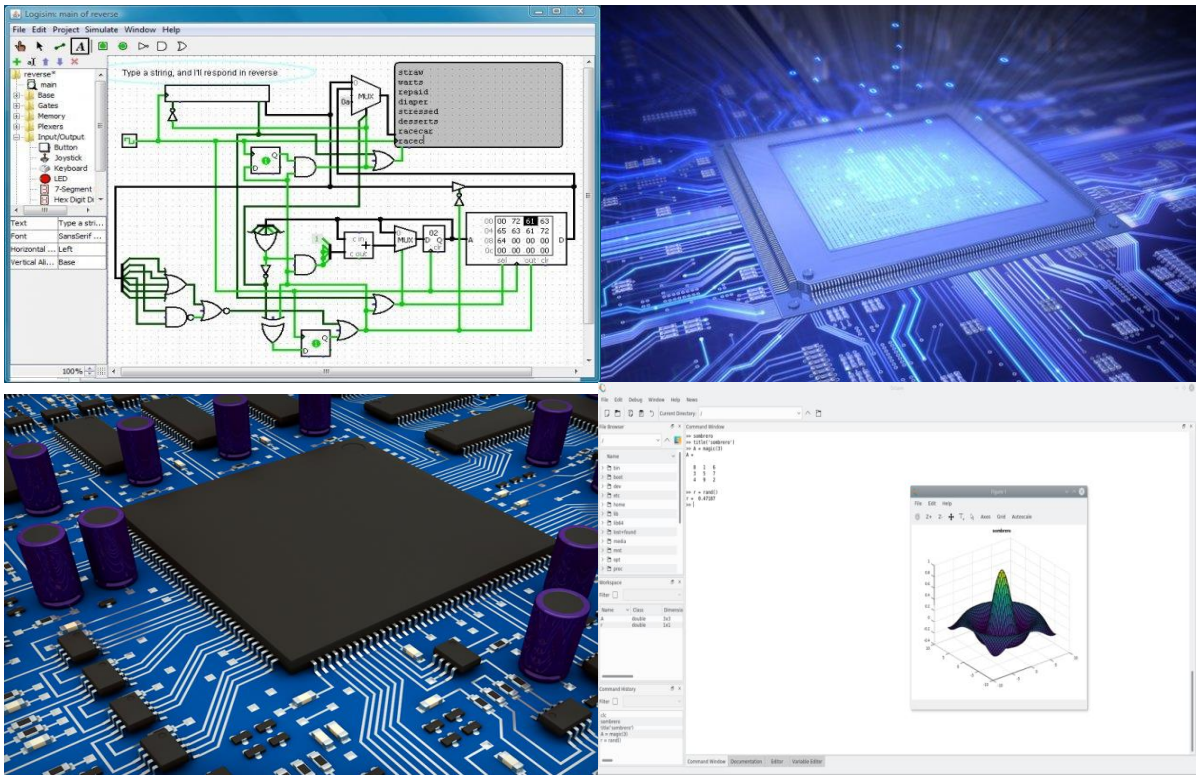
Curriculum & Contents

M. Tech.

(VLSI and Embedded Systems)



विश्वजीवनामृतं ज्ञानम्

ABV-Indian Institute of Information Technology & Management, Gwalior

June 2019

Name of the program -- M. Tech. (VLSI and Embedded Systems)

Semester I				
S. No.	**Subject Code**	**Title of the course**	**L-T-P**	**Credits**
1	MTES-6101	MOS VLSI Circuit Design	3-0-0	3
2	MTES-6102	CAD Algorithms	3-0-0	3
3	MTES-6103	Device Modelling and Simulation	3-1-0	4
4		Elective I	3-0-0	3
5		Elective II	3-0-0	3
6	MTES-6104	VLSI Circuit Lab	0-0-2	1
7	MTES-6105	CAD Lab	0-0-2	1
8	MTHS-6101	Professional Ethics	0-0-2	1
9	MTES-6106	Generic Computing		Audit
			Total credits	**19**

Semester II				
S. No.	**Subject code**	**Title of the course**	**L-T-P**	**Credits**
1	MTES-6201	Mixed Signal Design	3-0-0	3
2	MTES-6202	Embedded System Design	3-0-0	3
3		Elective I	3-0-0	3
4		Elective II	3-0-0	3
5	MTHS-6201	Research Methodology	3-0-0	3
6	MTES-6203	Analog Circuit Lab	0-0-4	2
7	MTES-6204	Embedded Lab	0-0-2	1
			Total credits	**18**

Semester III				
S. No.	**Subject code**	**Title of the course**	**L-T-P**	**Credits**
1		Elective-I	3-0-0	3
2	MTHS-7101	Technical Writing	0-0-2	1
3	MTES-7101	Seminar	0-0-2	1
4	MTES-7199	Major Project part I		6
			Total credits	**11**

Semester IV				
S. No.	**Subject Code**	**Title of the course**	**L-T-P**	**Credits**
1	MTES-7299	Major Project part II		12
			Total credits	**12**

List of Electives for VLSI and Embedded Systems

List of Electives for Semester I

S. No.	Subject Code	Course	L-T-P	Credits
1.	MTES-9101	Integrated Circuit Technology	3-0-0	3
2.	MTES-9102	VLSI Design	3-0-0	3
3.	MTES-9103	Synthesis of Digital System	3-0-0	3
4.	MTES-9104	VLSI Digital Signal Processing Systems	3-0-0	3

List of Electives for Semester II

S. No.	Subject Code	Course	L-T-P	Credits
1.	MTES-9201	VLSI Testing and Testability	3-0-0	3
2.	MTES-9202	Nanoelectronics	3-0-0	3
3.	MTES-9203	Memory Design	3-0-0	3
4.	MTES-9204	Analog IC design	3-0-0	3
5.	MTES-9205	VLSI Architecture	3-0-0	3
6.	MTES-9206	Hardware Security	3-0-0	3
7.	MTES-9207	VLSI Physical Design Automation	3-0-0	3

List of Electives for Semester III

S. No.	Subject Code	Course	L-T-P	Credits
1.	MTES-9301	Energy Aware Computing	3-0-0	3
2.	MTES-9302	Low Power VLSI Design	3-0-0	3
3.	MTES-9303	Spintronics: Principles and Devices	3-0-0	3
4.	MTES-9304	System Level Design and Modelling	3-0-0	3
5.	MTES-9305	Hardware Software Co-design	3-0-0	3

Please note:

a) The course contents are indicative in nature. Actual contents followed may deviate based on students/faculty interests.

b) Typically the evaluation is based on various components such as Minors (In-semester tests), Major examination (End-semester test), assignments, term papers, quizzes, presentations and class participation. The weightages for these components will be decided by the respective course instructors.

Semester I

1	**Code of the subject**	MTES-6101
2	**Title of the subject**	MOS VLSI Circuit Design
3	**Any prerequisite**	NIL
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Prof. Manisha Pattanaik
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	This course aims to convey knowledge of basic concepts of circuit design for digital VLSI components in state-of-the-art MOS technologies. Emphasis is on the circuit design, optimization, and layout of very high speed, high density or low power circuits for use in applications such as processors, signal and memory and periphery. Special attention will devoted to the most important challenges facing digital circuit designers today and in the coming decade, being the impact of scaling, deep submicron effects, interconnect, signal integrity, power distribution and consumption, and timing.
8	**Brief Contents (module wise)**	On completion of this course, students should have obtained a sound understanding of MOSFET device operation and the VLSI design methodology. Through this course, students should have gained the skills in the identification, formulation, and solution of problems relating to the design of MOS combinational and sequential logic circuits. They should be able to apply their knowledge of electronics and engineering in the design of CMOS integrated circuits and digital VLSI systems. **Detailed Class Schedule** This schedule is tentative and will be updated on a regular basis - **Module I: Introduction and Future Prospects** **Module II: Evolution of MOS Transistor Structure:** Structure and Operation of MOS, I~V Characteristics **Module III: Modeling of Transistor using SPICE:** Basic Concepts, The Level 1 Model Equations, The Level 2 Model Equations, The Level 3 Model Equations, State–of –the-art MOSFET Models, Capacitance Models, Comparison of SPICE Models, Capacitance Models, Comparison SPICE MOSFET Models, Typical SPICE Model Parameters **Module IV: MOS Inverters Static Characteristics:** Resistive Load Inverter, Inverters with n-type MOSFET Load, CMOS Inverter, and Exercise Problems **Module V: MOS Inverters: Switching Characteristics and Interconnect Effects** Delay-Time Definitions, Calculation of Delay Times, Inverter Design with Delay Constraints, Estimation of Interconnect Parasitics, Calculation of Interconnect Delay, Switching Power Dissipation of CMOS Inverters, Super Buffer Design **Module VI: Combinational MOS Logic Circuits:** MOS Logic Circuits with depletion NMOS Loads, CMOS Logic Circuits, Complex Logic Circuits, CMOS Transmission Gates (Pass Gates), and Exercise Problems **Module VII: Sequential MOS Logic Circuits:** Behavior of Bistable Elements, SR Latch Circuit, Clocked Latch and Flip Flop Circuit, CMOS D-Latch and Edge-Triggered Flip Flop, and Exercise Problems

		Module VIII: Dynamic Logic Circuits Basic Principles of Pass Transistor Circuits, Dynamic CMOS Circuit Techniques, High Performance Dynamic CMOS Circuits, and Exercise Problems **Module IX: Semiconductor Memories:** Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), Nonvolatile Memory, Flash Memory, and Exercise Problems. **Module X: Low Power CMOS Logic Circuits:** Overview of Power Consumption, Low Power Design through Voltage Scaling, Estimation and Optimization of Switching Activity, Reduction of Switched Capacitance, and Exercise Problems
9	**Contents for lab (If applicable)**	NIL
10	**List of text books/references**	Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and design, Third Edition, Tata McGraw-Hill , 2003. Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Prentice Hall of India, Second Edition, 2003. Neil H. E. Weste and K. Eshraghian, Principles of CMOS VLSI Design, Second Edition, Pearson Education Asia, 2002. Wayne Wolf, Modern VLSI Design: System-on-Chip Design, Third Edition, Pearson Education Asia 2003. Ivan Sutherland, R. Sproull and D. Harris, "Logical Effort: Designing Fast CMOS Circuits", Morgan Kaufmann. **Other readings** Journal of Solid State Circuits IEEE International Conference proceedings and Journals in VLSI Circuits and Slide Supplements Symposium on VLSI Circuits, Systems and Digests of Technical Papers International Symposium on Low Power Electronic Design

1	**Code of the subject**	MTES-6102
2	**Title of the subject**	CAD Algorithms
3	**Any prerequisite**	Digital Design, Data Structures and Algorithms
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Prof. G.K. Sharma
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	The main objective of this course is to provide in-depth understanding of the theoretical as well as practical concepts of the designing algorithms for CAD tools for VLSI design. The students will be able to identify and develop new algorithms and CAD tools for VLSI design. The scope of this course is also to visualize new Design Automation (DA) research problems in view of the challenges of designing multi-core and/or many-core system-on-chip in the nanometer regime. Another objective of this course is to give the exposure to machine learning and deep learning algorithms for designing efficient hardware in IoT era.
8	**Brief Contents (module wise)**	**Unit I: Introduction to VLSI-CAD:** VLSI design flow, Gasjki's Y-chart, challenges, motivating factors and recent trends in design automation research. VLSI design styles: full-custom, standard-cell, gate-array, macro-cell, module generation, PLAs and FPGAs. **Unit II: Digital hardware modeling:** Logic and system level modeling, functional and structural models, level of modeling, hardware description languages, benchmark circuits (ISCAS'85, ISCAS'89…). **Unit III: Simulation algorithms design verification:** Types of simulation, complied code simulation, event-driven simulation, delay models, gate-level event-driven simulation, design and development of simulation tools, graph data structure and algorithms for VLSI-CAD. **Unit IV: High-level synthesis:** Logic synthesis, high-level synthesis design flow, design capture, data and control graph generation, resource allocation, operation scheduling algorithms, ASAP, ALAP, resource occupancy, mobility, time constraints and resource constraints scheduling, resource binding, data life-time, left-edge algorithm, task to agent problem, function unit binding, port binding, data path and control path generation. **Unit V: Algorithms for physical design automation:** Circuit partitioning: deterministic and stochastic algorithms for circuit portioning, Kernighan-Lin algorithm and simulated annealing. Floor-planning: model and cost functions, slicing and non-slicing floorplans, polar graphs and adjacency graphs for floorplans. Basic placement and routing algorithms. **Unit VI: Network-on-Chip (NoC):** Introducing NoC as a future SoC paradigm, NoC topologies, mapping of IPs, routing algorithms, CAD tool development for NoC designs, benchmarks for real-world applications such as multimedia system, telecom, office automation. **Unit VII: Machine Learning and Deep Learning Algorithms:** Supervised learning – Regression: Linear regression, Logistic regression; Classification – Support Vector Machines (SVM), Kernel methods, Decision trees, Ensemble learning, Model selection and Feature selection, Evaluation metrics; Clustering algorithms and Principal Component Analysis; Artificial Neural Networks, Convolutional Neural Networks and Generative Adversarial Networks; Case Study – Energy-Efficient hardware realization of Convolutional Neural Networks.

9	**Contents for lab (If applicable)**	Not applicable
10	**List of text books/references**	1. Giovanni De Micheli, *Synthesis and Optimization of Digital Circuits*, Tata McGraw Hill, 1994 2. D.D Gajski et al., *High Level Synthesis: Introduction to Chip and System Design*, Kluwer Academic Publishers, 1992 3. B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*. Oxford, U.K.: Oxford Univ. Press, 2000, pp. 93–96. 4. N. Zhu et. al. *Design of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing*. IEEE Trans. on VLSI systems, 18(8):1225 –1229, Aug. 2010. 5. A.B. Kahng and S. Kang, "Accuracy-configurable adder for approximate arithmetic designs," in *Proc. DAC*, pp. 820-825, 2012. 6. S.M. Sait and H. Youssef, "*VLSI physical design automation: theory and practice*", World Scientific Pub. Co., 1999. 7. Christopher Bishop, Pattern Recognition and Machine Learning, Springer International Edition. 8. Ian Goodfellow et al. Deep Learning, MIT press, 2015 9. Current Literature: *IEEE Trans. on CAD of ICs, IEEE Trans. on VLSI Systems, ACM TODAES, Proceedings IEEE, DAC, DATE, ICCAD, ICCD, ASP-DAC, VLSID*

1	**Code of the subject**	MTES-6103
2	**Title of the subject**	Device Modelling and Simulation
3	**Any prerequisite**	VLSI Design, Electronics Devices and Circuits
4	**L-T-P**	3-1-0
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	➢ The objective of the course is to provide the fundamental knowledge for understanding concepts of semiconductor devices. ➢ Upon successful completion of the course, students will be able to grasp fundamental knowledge of semiconductor devices for Integrated Circuit design. ➢ Be able to model the devices using SPICE modeling.
8	**Brief Contents**	**M I: Device Modeling:** Overview of MOS transistor physics, Two-Terminal MOS structure, Flat -band voltage, Effect of Gate-substrate voltage on surface condition, Inversion, Limitation of long channel analysis, short-channel effects: velocity saturation, device degradation, channel length modulation, body bias effect, threshold adjustment, mobility degradation, hot carrier effects, MOSFET scaling goals, gate coupling, velocity overshoot, high field effects in scaled MOSFETs, substrate current and effects in scaled MOSFETS. Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, Nonconventional MOSFET (FDSOI, SOI, Multi-gate MOSFETs). **M II: Simulation:** Introduction to SPICE modeling, modeling of resistor, capacitor, inductor, diode, BJT, JFET, MOSFET, model parameters, Brief overview of BSIM and EKV model, Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations –MOSFETs and SOI (Device and process simulator), Importance of semiconductor device simulators -Key elements of physical device simulation, historical development of the physical device modeling.
9	**Contents for lab (If applicable)**	TCAD Simulator, Spice Simulator.
10	**List of text books/references**	1. Y. Tsividis, “Operation and modeling of MOS transistors”, 2nd Edition, McGraw-Hill, 1999. 2. Paul W. Tuinenga, “SPICE: A Guide to Circuit Simulation and Analysis Using PSpice”, 3rd Edition, Pearson, 2006. 3. Paolo Antognetti and Giuseppe Massobrio, “Semiconductor Device Modeling with SPICE”, 2ndEdition, Tata McGraw-Hill, 2010. 4. BSIM Model (http://www-device.eecs.berkeley.edu/bsim/) 5. S. M. Sze and M.K. Lee, “Semiconductor devices-Physics and Technology”, 3rd Edition, John Wiley & Sons, 2012. 6. V. Vasileska, S. M. Goodnick, and Gerhard Klimeck , “Computational Electronics: Semiclassical and Quantum Device Modeling and Simulation”, CRC Press, 2010 7. P. Colinge, “FinFETs and Other Multi-Gate Transistors”, Springer, 2009.

1	**Code of the subject**	MTES-6104
2	**Title of the subject**	VLSI Circuit Lab
3	**Any prerequisite**	Digital and Analog VLSI Design
4	**L-T-P**	0-0-2
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	➢ To educate students with the knowledge of Verilog coding and test bench. ➢ Students will be able to compile, simulate and synthesize the Verilog code. ➢ From this lab the students will be able to draw the schematic diagram and layout for the inverter & digital gates and verify their functionality
8	**Brief Contents**	**M I:** Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with the technological library, with the given Constraints. Do the initial timing verification with gate level simulation. ➢ An inverter ➢ A Buffer ➢ Transmission Gate ➢ Basic/universal gates ➢ Flip flop -RS, D, JK, MS, ➢ Serial & Parallel adder ➢ 4-bit counter (Synchronous and Asynchronous counter) **M II:** Design an Inverter with given specifications, completing the design flow mentioned below: ➢ Draw the schematic and verify the following: i) DC Analysis ii) Transient Analysis ➢ Draw the Layout and verify the DRC, ERC. ➢ Check for LVS. ➢ Extract RC and back annotate the same and verify the Design. ➢ Verify & Optimize for Time, Power and Area to the given constraint.
9	**Contents for lab (If applicable)**	Mentioned above.
10	**List of text books/references**	1. M. Morris Mano, "Digital Logic and Computer Design", Pearson Prentice Hall, 2008. 2. Jayaram Bhasker, "A *VHDL* Primer", Prentice Hall, 3rd edition, 2009. 3. D. FitzPatrick, I. Miller, "Analog Behavioral Modeling with the Verilog-A Language", Springer; 1998 edition. 4. T.R. Padmanabhan, B. Bala Tripura Sundari, "Design through Verilog HDL", Wiley, 2008. 5. M. Morris Mano, "Digital Design: with an Introduction to the Verilog Hdl", Pearson Education, 5th edition, 2014. 6. Jayaram Bhasker, "A Verilog Hdl Primer", BS Publications/bsp Books, 2008. 7. S. M. Kang, Y. Leblebici "CMOS Digital Integrated Circuits: Analysis and Design", McGraw Hill Education; 3 edition, 2002.

1	**Code of the subject**	MTES-6105
2	**Title of the subject**	CAD Lab
3	**Any prerequisite**	Nil
4	**L-T-P**	0-0-2
5	**Name of the proposer**	Dr. SUNIL KUMAR and Dr. SOMESH KUMAR
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	After successful completion of this lab course, students will able to understand basic CAD commands, tools, multi-view drawing and dimensioning techniques. Additionally, students will gain the ability of manipulate drawings, drawing projections, understanding Section and Auxiliary Views etc.
8	**Brief Contents (module wise)**	**Module-I**: Overview of Linux operating System, Shell Programming **Module-II:** Verification-High level synthesis -Compaction. Physical Design Automation of FPGAs, MCMS-VHDL- Verilog-Implementation of Simple circuits using VHDL and Verilog & System C. **Module-III:** Designing Datapath Elements in Digital Circuits **Module-IV:** Design of Finite State Machines
9	**Contents for lab (If applicable)**	
10	**List of text books/references**	1. Red Hat Linux Administration: A Beginner's Guide 2. Jayaram Bhasker, "A VHDL Primer", Prentice Hall, 3 rd edition, 2009. 3. D. FitzPatrick, I. Miller, "Analog Behavioral Modeling with the Verilog-A Language", Springer; 1998 edition. 4. T.R. Padmanabhan, B. Bala Tripura Sundari, "Design through Verilog HDL", Wiley, 2008. 5. M. Morris Mano, "Digital Design: with an Introduction to the Verilog Hdl", Pearson Education, 5 th edition, 2014. 6. Jayaram Bhasker, "A Verilog Hdl Primer", BS Publications/bsp Books, 2008. Jayaram Bhasker, "A System C Primer ", 7. HDL Chip Design: A Practical Guide for Designing, Synthesizing and Simulating ASICs and FPGAs Using VHDL or Verilog, Douglas J. Smith, Doone Publications

1	**Code of the subject**	MTHS-6101
2	**Title of the subject**	Professional Ethics
3	**Any prerequisite**	Nil
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Prof. V.S.R. Krishnaiah
6	**Will this course require visiting faculty**	Yes
7	**Learning Objectives of the subject (in about 50 words)**	The primary objective of this course is to sensitize students on the concept of Ethics and Human Values and make them understand the relevance of these ideas in their day to day personal and professional lives. The Course aims to instill moral and social values as well as professional code of conduct in the students to make them good quality professionals so as to perform their professional responsibilities better in their future career.
8	**Brief Contents (module wise)**	**Module-I:** Definitions of Ethics, Engineering Ethics, and Morality. Categorization of Ethics, Differentiation of Morality and Ethics, Ten personal ethical behaviors which are globally acceptable, Definition of virtues, Elaboration of cardinal virtues, Definition of human values, Shalome H Shwartz value classification with examples **Module-II:** Definition of Profession and Professional, Responsibilities of professionals, the objectives of any one professional association, ACM Code of Ethics and Professional Conduct, IEEE Code of Ethics **Module-III:** Significance of ethics in ICT sector, Global Ethical Issues in ICT Sector with examples, Definitions of CSR, The stakeholders and their expectations from an organization, The Company Act 2013, Benefits of CSR in organization, Examples of CSR in ICT sector **Module-IV:** Definition of Emotional intelligence, Importance of Emotional intelligence for Professionals, Five elements of Emotional intelligence, Significance of EI for professional success with examples, Ethical Dilemmas, Main features of Whistle Blowing, Preparation for Professionals and CEOs for avoiding unethical issues in their organizations.
9	**Contents for lab**	Not Applicable
10	**List of text books/references**	1.Professional Ethics by R.Subramanian, Oxford University Press, 2013 2. Working with Emotional Intelligence by Daniel Goleman, Bloomsbury, 2004

1	**Code of the subject**	MTES-6106
2	**Title of the subject**	Generic Computing
3	**Any prerequisite**	NA
4	**L-T-P**	Audit
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	At the end of the course the student will be able to: ➢ Formulate problem in terms of finite element. ➢ Estimate the error in the method he uses ➢ Generate the grid required for the problem ➢ Apply FEM, FVM methods to analyse ICs.
8	**Brief Contents**	**M I: Numerical solution of differential equations:** FEM, FVM, FDM. **M II: Linear circuit simulation techniques:** Forward Euler Approximation, Backward Euler Approximation, Trapezoidal Approximation, One Step Integration Approximation **M III: Non-linear circuit simulation techniques:** Non Linear DC analysis, Newton RaphsonIteration, Multi-Dimensional Newton RaphsonIteration. Error estimates, Transient and small signal solutions, Applications to device and process simulation, Layout algorithms, Yield estimation algorithms, Symbolic analysis and Synthesis of Analog ICs. **M IV: Introduction to physical design :** VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles.
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	1. L. O. Chua and P. M. Lin, Computer Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques, Prentice Hall, 1975. 2. Pallage, R. Rohrer and C. Visweswaraiah, Electronic Circuit and System Simulation Methods, McGrawHill, 1995. 3. Naveed Shewani, Algorithms for VLSI Physical Design Automation, 3rd Edition, Kluwer Academic, 1999.

Semester II

1	**Code of the subject**	MTES6201
2	**Title of the subject**	Mixed Signal Design
3	**Any prerequisite**	NIL
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Gaurav Kaushal
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	The objective of the Mixed Signal Design is to acquaint the students with basic CMOS analog building blocks and analog sub-system design. The subject gives the platform for design and analyzes the CMOS analog circuits.
8	**Brief Contents (module wise)**	Necessity and advantages of CMOS Analog Circuits; Overview of MOS amplifiers and their analysis; Differential amplifier; Current mirrors; Frequency response; two stage CMOS op-amp; calculation of overall gain and rout; determination of dominants poles; compensation and relocation of poles and zeros; Feedback; Bandgap References; Oscillators
9	**Contents for lab (If applicable)**	Separate Lab "Analog Circuit Lab" is provided as 1 credit.
10	**List of text books/references**	1) B. Razavi, Design of Analog Integrated Circuits, McGraw Hill Education, 2018. 2) P. E. Allen, D. R. Holberg, CMOS Analog Circuit Design, 3rd Edition, Oxford University Press, 2013.

1	Code of the subject	MTES-6202
2	Title of the subject	Embedded System Design
3	Any prerequisite	NIL
4	L-T-P	3-0-0
5	Name of the proposer	Prof. Manisha Pattanaik
6	Will this course require visiting faculty	No
7	Learning Objectives of the subject (in about 50 words)	This course aims at developing knowledge and skills in Embedded System Design and offers strong knowledge in Embedded System Design covering thrust areas such as Advanced Embedded Microcontrollers, Embedded processors and Interface standards, Real Time Embedded Systems, Advanced Embedded System Design and System on Chip.
8	Brief Contents (module wise)	**Detailed Class Schedule** This schedule is tentative and will be updated on a regular basis - **Module I:** Introduction to Embedded Systems and Embedded Processors **Module II:** Embedded system architecture, classifications of embedded systems, challenges and design issues in embedded systems, fundamentals of embedded processor and microcontrollers, CISC vs. RISC. **Module III:** Introduction to PIC microcontrollers, PIC architecture, comparison of PIC with other CISC and RISC based systems and microprocessors, memory mapping. **Module IV:** 8051 I/O ports, I/O bit manipulation programming, timers/counters, programming to generate delay and wave form generation, I/O programming, LEDs, 7segment LED, LCD and Keypad interfacing. **Module V:** Basic design using RTOS, Real time operating systems, Kernel architecture: Hardware, Task/process scheduling, Embedded operating systems, Task scheduling in embedded systems: task scheduler, first in first out, shortest job first, round robin. **Module VI:** Bus architectures and transactions, Serial interconnects, Networked embedded systems: Bus protocols, I2C bus and CAN bus. Hands-on Training with ARM Processors
9	Contents for lab (If applicable)	NIL
10	List of text books/references	1. Embedded Systems Architecture Programming and Design by Raj Kamal, Second Edition, Tata MC Graw-Hill, 2008. 2. Designing Embedded Systems with PIC Microcontrollers: principles and applications, Tim Wilmshurst, Second Edition, Elsevier, 2005. 3. Embedded Systems Design, Steve Heath, Second Edition, Newnes, 2002.

1	**Code of the subject**	MTHS-6201
2	**Title of the subject**	Research Methodology
3	**Any prerequisite**	No
4	**L-T-P**	3-0-0 3 credit
5	**Name of the proposer**	Dr. Pankaj Srivastava
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	To enable researchers (Ph.D., MTech students), irrespective of their discipline, in developing the most appropriate methodology for their research studies. To make them familiar with the art of using different research methods and techniques
8	**Brief Contents (module wise)**	**RESEARCH FUNDAMENTALS:** Research, types of research, Research vs research methods, Research process, Relevant and quality research. Problem-solving in engineering, Identification of research topic, Problem definition, Literature survey, literature survey, Literature review, Research Design. **MATHEMATICAL MODELLING & SIMULATION:** Models in general, Mathematical models, Model classifications, Modeling of engineering systems Theoretical models, Empirical models, Model evaluation, Limitations of mathematical models. Simulation models, Steps in a simulation study, Simulation software, Validation and data collection, Applications. **HYPOTHESES TESTING , ANALYSIS & SCALING TECHNIQUES:** Formulation of Hypothesis, Testing of hypothesis, Analysis of variance, Design of experiments, Multivariate analysis, Simple regression and correlation, measurement & scaling techniques. **ANALYSIS AND INTERPRETATION OF DATA:** Data checking, Data analysis, Statistical, Graphical and Numerical data analysis, Interpretation of results in research , need for Interpretation, Accuracy, Precision, Uncertainty and variability, Repeatability and reproducibility, Error definition and classification, Analysis of errors, Statistical analysis of errors. **SKILLS AND ETHICS IN RESEARCH:** Basic communication model, Preparing papers for journals, synopsis of research work, Reference citation, Listing of References. Thesis writing, Steps in writing the report, presentation of graphs, figures, tables, Structure of thesis report, main body of thesis, summary, references, Evaluation of a thesis, Ethics in research, Intellectual property rights, copyright laws, Patent rights.
9	**Contents for lab (If applicable)**	Introduction to LaTex software. Practical applications of SPSS, ANOVA Applications and case studies of parametric and non-parametric tests
10	**List of text books/references**	1. Research Methodology- C R Kothari, New Age International. 2. Research Methodology: A step by step guide for beginners- Ranjit Kumar, Sage Publications. 3. Guide to Research & Documentation- Kirk G. Rasmussen, Prentice Hall. 4. Research Methods- R. Panneerselvan, Prentice Hall 5. Research Methodology for Engineers- R Ganeshan, MJP Publishers

1	**Code of the subject**	MTES-6203
2	**Title of the subject**	Analog Circuit Lab
3	**Any prerequisite**	Digital and Analog VLSI Design
4	**L-T-P**	0-0-4
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	➢ From this lab the students will be able to draw the schematic diagram and layout for the inverter, op-amp and amplifiers and verify their functionality. ➢ Understand the significance of different biasing styles and apply them for different circuits. ➢ Design all basic building blocks like sources, sinks, mirrors, up to layout level.
8	**Brief Contents**	**M I:** Design an Inverter with given specifications, completing the design flow mentioned below: ➢ Draw the schematic and verify the following: i) DC Analysis ii) Transient Analysis ➢ Draw the Layout and verify the DRC, ERC. ➢ Check for LVS. ➢ Extract RC and back annotate the same and verify the Design. ➢ Verify & Optimize for Time, Power and Area to the given constraint. **M II:** Design a Common source and Common Drain amplifier with given specifications, completing the design flow mentioned below: ➢ Draw the schematic and verify the following: i) DC Analysis ii) Transient Analysis ➢ Draw the Layout and verify the DRC, ERC. ➢ Check for LVS. ➢ Extract RC and back annotate the same and verify the Design. ➢ Verify & Optimize for Time, Power and Area to the given constraint. **M III:** Design a single stage differential amplifier, operational amplifier with given specifications, completing the design flow mentioned below: ➢ Draw the schematic and verify the following: i) DC Analysis ii) Transient Analysis ➢ Draw the Layout and verify the DRC, ERC. ➢ Check for LVS. ➢ Extract RC and back annotate the same and verify the Design. ➢ Verify & Optimize for Time, Power and Area to the given constraint.
9	**Contents for lab (If applicable)**	Mentioned Above.
10	**List of text books/references**	1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, Inc., New York, USA. 2. R. J. Baker, H W Li, D. E. Boyce, "CMOS Circuit design, Layout and Simulation", PHI EEE. 3. Neil H. E. Weste, Kamran Eshraghian, "Principles of CMOS VLSI Design", Addison Wesley. 4. "Basics of CMOS Cell Design", Etienne Sicard. 5. "CIRCUIT DESIGN for CMOS VLSI", John P. Uyemura 6. "CMOS Digital Integrated Circuits: Analysis and Design," Sung-Mo Kang And Yusuf Leblebici.

1	**Code of the subject**	MTES-6204
2	**Title of the subject**	Embedded Lab
3	**Any prerequisite**	NA
4	**L-T-P**	0-0-2
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	➢ Learn assembly language programming & embedded. ➢ Learn and design embedded systems and real-time systems. ➢ Define the unique design problems and challenges of real-time systems ➢ Identify the unique characteristics of real-time operating systems and evaluate the need for real-time operating system. ➢ Explain the general structure of a real-time system ➢ Know and use RTOS to build an embedded real-time system. ➢ Gain knowledge and skills necessary to design and develop embedded applications based on real-time operating systems.
8	**Brief Contents**	**List of Experiments:** 1. Write an ALP for all ALU operations in 8051. 2. An assembly language program to generate 10 KHz frequency using interrupts on P1.2. 3. Write an ALP to generate square of 10 KHz using Timer 0. 4. To display a string (ABV-IIITM Gwalior) on LCD. 5. An ALP to interface seven segment with 8051 and display 0-9 on it. 6. Write an ALP to interface 4x4 keyboard with 8051. 7. Write a program to show the use of INT0 and INT1 of 8051. 8. Write a program for temperature & to display on intelligent LCD display. 9. Write a program to generate a Ramp waveform using DAC with micro controller. 10. Arduino and Raspberry Pi Microcontroller based Projects.
9	**Contents for lab (If applicable)**	Mentioned above.
10	**List of text books/references**	1. H. Boyet, and R. Katz, “8051-Programming, Interfacing, Applications: 81 Hands-On Experiments with Intel's SDK-51”, BPB publications. 2. The 8051 Microcontroller and Embedded Systems: Using Assembly and C by Mazidi. 3. Embedded Systems Design: An Introduction to Processes, Tools & Techniques by Arnold S. Berger

Semester III

1	**Code of the subject**	MTHS-7101/MTIS-7101
2	**Title of the subject**	Technical Report Writing
3	**Any prerequisite**	-
4	**L-T-P**	0-0-2
5	**Name of the proposer**	Dr. Arun Kumar
6	**Will this course require visiting faculty**	Yes
7	**Learning Objectives of the subject (in about 50 words)**	➢ To learn written communication skills in the wake of present day professional world ➢ To enhance the understanding of written communication with practice oriented approach ➢ To collect, analyze and report data ➢ To familiarize with grammar and usage ➢ To acquire higher order writing skills through project assignments
8	**Brief Contents (module wise)**	➢ Fundamentals of communication ➢ Elements of Report writing ➢ Types of reports such as memo, corrigendum ➢ Technical reports ➢ Sources of data ➢ Data analysis ➢ Illustrating data ➢ Mechanics of writing ➢ Report structure ➢ Oral presentation ➢ Issues related to plagiarism and ways to counter the same
9	**Contents for lab (If applicable)**	➢ Data Analysis ➢ Report writing ➢ Report presentation
10	**List of text books/references**	1. Sharma, R.C. and K. Mohan, Business Correspondence and Report Writing, Tata McGraw Hill, 5th edition, 2016. 2. Gerson, Sharon J and Stern M. Gerson, Technical Writing: Process and Product, Pearson, 3rd edition, 2000

1	**Code of the subject**	MTES-7101
2	**Title of the subject**	Seminar
3	**Any prerequisite**	NA
4	**L-T-P**	0-0-2
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	➢ To expose students to the 'real' working environment and get acquainted with the organization structure, business operations and administrative functions ➢ To promote and develop presentation skills and import a knowledgeable society. ➢ To set the stage for future recruitment by potential employers. ➢ Students will be able to apply a multidisciplinary strategy to address current, real-world issues.
8	**Brief Contents**	**Broad areas :** Algorithms for Physical Design, Device Modelling, SERDES, Clock Tree Building Schemes, MRAMS, Low Power Architectures, Interconnects, Graphene Based Devices, Hybrid Interconnects, FinFETs, Nano-RAM, On chip ESD protection strategies for RF circuits in CMOS technologies, Trend and challenge on SOC design, Deep Learning, Moore's Law, 3D ICs, Nanomaterial, Nanofabrication etc.
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	➢ https://ieeexplore.ieee.org/Xplore/home.jsp ➢ https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6210560 ➢ https://www.ieee.org/conferences/organizers/planning-presentation-of-papers.html

List of Electives for Semester I

1	**Code of the subject**	MTES9101
2	**Title of the subject**	Integrated Circuit Technology
3	**Any prerequisite**	NIL
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Gaurav Kaushal
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	This course will introduce the student to the world of semiconductor IC technology fabrication. The course will also provide a comprehensive flavor of advanced device fabrication techniques, the effect of parasitics and process variations on device performance.
8	**Brief Contents (module wise)**	Modern Semiconductor IC fabrication Industrial/Academic Landscape; Overview of modern CMOS process flow – basic steps; Lithography; Oxidation; Si and SO_2 interface; Electrical measurement; MOS capacitor; Diffusion; Ion-Implantation; Effects of device parasitic and process variations on device and circuit performance; Advanced device fabrication
9	**Contents for lab (If applicable)**	No
10	**List of text books/references**	1) Plummer, Deal, Griffin, Silicon VLSI Technology: Fundamentals, Practice, and Modeling, 1,Prentice Hall, 2000. 2) Gandhi, S. K., "VLSI Fabrication Principles: Silicon and Gallium Arsenide", John Wiley and Sons, 2003.

1	**Code of the subject**	MTES-9102
2	**Title of the subject**	VLSI Design
3	**Any prerequisite**	NIL
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Prof. Manisha Pattanaik
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	The main objective of this course is to provide in-depth understanding of the VLSI Design flow, applications of CAD tools and timing simulations. Students will be exposed to the state-of-the-art CAD tools and CMOS circuit and system design and implementation methods.
8	**Brief Contents (module wise)**	**Detailed Class Schedule** This schedule is tentative and will be updated on a regular basis - **Module I: Introduction to VLSI Systems:** VLSI overview, VLSI designs flow, design hierarchy, VLSI design styles. Semiconductor technology trends and impact on VLSI architecture and design; **Module II: Methodologies for VLSI structured design:** Design analysis and simulation, Design Verification, Implementation approaches, Design synthesis, Validation and testing of integrated circuits. **Module III: VLSI system design and optimizations for performance and power Design for Test Case Studies:** Application of Tools to design VLSI system based on above concepts. Students will use VLSI CAD tools and programmable devices for ASIC and FPGA implementation. The course assignment will focus on layout analysis, computer-aided layout, and logic and timing simulation.
9	**Contents for lab (If applicable)**	NIL
10	**List of text books/references**	"Principles of CMOS VLSI Design", Neil H. E. Weste, Kamran Eshraghian, Addison Wesley, 1993. "CMOS Digital Integrated Circuits: Analysis and Design," Sung-Mo Kang And Yusuf Leblebici, 2005. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", Third Edition, Prentice-Hall of India, 1995. Eshraghian, K., Pucknell, D.A. and Eshraghian, S., "Essentials of VLSI Circuit and System", Second Edition, Prentice-Hall of India, 2005. Uyemera, P.J., "Introduction to VLSI Circuits and Systems", Fourth Edition, John Wiley & Sons, 2005. Donald G. Givone "Digital Principles and Design", Tata McGraw-Hill, 2002. Roth, Charles H., "Digital System Design using VHDL", Thomson Learning, 1998. Stephen Brown and Zvonk Vranesic., "Fundamentals of Digital Logic with VHDL Design" Tata McGraw-Hill, 2002.

1	**Code of the subject**	MTES9103
2	**Title of the subject**	Synthesis of Digital System
3	**Any prerequisite**	Data Structures and Digital Circuit Design
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. SUNIL KUMAR
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	After successful completion of this course, students will able to understand techniques for digital system behavioural synthesis, verification and performance evaluation. Analysis and synthesis of modern System-on-Chip design methods are the main goal of this course.
8	**Brief Contents (module wise)**	Module-I Review of hardware description languages and VHDL, Behaviour and Structure of VHDL. Data and control flow repre- sentations, Data flow graph (DFG) and Control data flow graph (CDFG) descriptions Module-II Introduction to High-level Synthesis: Design space ex- ploration, Constructive vs. transformational/iterative techniques, Be- havioural optimisation, Scheduling, allocation, module binding and controller synthesis, Register Allocation and Timing Issues. Module-III Finite State Machine Synthesis, Logic Synthesis and Binary Decision Diagrams, Scheduling and binding algorithms. Module-IV Technology Mapping, Timing Analysis,and Physical Synthesis, Design for Testability, on-line test.
9	**Contents for lab (If applicable)**	No
10	**List of text books/references**	1. Giovanni de Micheli, Synthesis and Optimization of Digital Circuits, McGraw Hill 2. Morris Mano and Michael D. Ciletti, "Digital Design", 4thEd., Pearson Education, 2008 3. C.H. Roth, "Fundamentals of Logic Design", 5th Ed.,Cengage Learning, 2004.

1	**Code of the subject**	MTES-9104
2	**Title of the subject**	VLSI Digital Signal Processing Systems
3	**Any prerequisite**	Digital Signal Processing
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Vinal Patel
6	**Will this course require visiting faculty**	NA
7	**Learning Objectives of the subject (in about 50 words)**	➢ Design and optimize VLSI architectures for basic DSP algorithms. ➢ Comprehend various sources of errors in implementation of DSP algorithms and device means to control them while implementing the DSP systems as per the specifications demanded by applications.
8	**Brief Contents (module wise)**	**Module I:** Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital Filters, Parallel Processing. Pipelining and Parallel Processing for Low Power. Retiming: Introduction, Definition and Properties, Solving System of Inequalities, Retiming Techniques. **Module II:** Unfolding: Introduction an Algorithms for Unfolding, Properties of Unfolding, Critical Path, Unfolding and Retiming Application of Unfolding. Folding: Introduction to Folding Transformation, Register Minimization Techniques, Register Minimization in Folded Architectures, Folding in Multirate Systems. **Module III:** Systolic Architecture Design: Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations Containing Delays. **Module IV:** Fast Convolution: Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	1. Parhi, Keshab K. VLSI digital signal processing systems: design and implementation. John Wiley & Sons, 2007. 2. Kung. S.Y., H.J. While house T. Kailath, VLSI and Modern signal processing, Prentice Hall, 1985.

List of Electives for Semester II

1	**Code of the subject**	MTES-9201
2	**Title of the subject**	VLSI Testing and Testability
3	**Any prerequisite**	VLSI Design, CAD Algorithms
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Prof. G.K. Sharma
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	The main objective of this course is to provide in-depth understanding of the problems encountered in testing large circuits, approaches to detect and diagnose the faults and methods to improve the design to make it testable. The students will be able to develop algorithms and tools for VLSI testing, designing of testable and trustworthy circuits. The scope of this course is to particularly address the challenges in the VLSI testing domain and get motivated towards research in this field.
8	**Brief Contents (module wise)**	**Unit I: Introduction and Fault Modeling:** Testing problem, economics of testing, approaches to testing, fault-analysis and fault-models, analysis at component level, gate level and functional block level. Physical fault model, stuck-at fault model, stuck-open and bridging fault-model. **Unit II: Testing Techniques:** Algebraic and structural testing methods, path sensitization, Boolean difference. Test Generation of Combinational Circuits: D-algorithm, PODEM, FAN, SOCRATES, static, dynamic and recursive learning. Test Generation of Sequential Circuits: Time frame expansion methods, forward-time, reverse-time, initialization and PSI problem, Fastest and Hitest. Parallel processing techniques for test generation, Boolean Satisfiability, transitive-closure based and Neural Network based approaches. **Unit III: Fault Simulation:** Serial, parallel, deductive and concurrent fault simulation, parallel- pattern single fault propagation method, hierarchical fault simulation. **Unit IV: Design for Testability and Built-in-self-test:** Controllability and observability measures, TEMEAS, SCOAP, ad-hoc design for testability techniques, full scan, partial scan and boundary scan techniques, built-in-logic-block-observer (BILBO), linear feedback shift register (LFSR), theory of LFSRs, pseudo-random and weighted random testing, built-in-self-test (BIST). **Unit V: Design for Trust Techniques:** Basic threats and vulnerabilities in combination and sequential digital design. Different Types of Attacks: Hardware Trojan (HT), IP Piracy and Overbuilding, Reverse Engineering, Side channel Analysis and Counterfeiting. Counter Measures for different types of attacks: Detection based approaches – Hardware Trojan Detection, Watermarking and Fingerprinting. Prevention based Approaches – Design-for-Trust Techniques such as Logic Encryption/Obfuscation and Camouflaging.
9	**Contents for lab (If applicable)**	Not applicable
10	**List of text books/references**	**1.** Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "*Digital System Testing and Testable Design*", IEEE Press and also available from Jaico Publication House, 2001. **2.** Michael L. Bushnell and Vishwani D. Agrawal, "*Essential of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*", Kluwer Academic Publishers, 2002. **3.** Dhiraj K. Pradhan, "*Fault-Tolerant Computing*", Vol. 1, Prentice-Hall, 1986. **4.** Instructor slides to be distributed in class. ***5.*** Research papers published in *IEEE Trans. on CAD of ICs, IEEE Design & Test of Computers, Proceedings IEEE, Test, DAC, DATE, ASP-DAC, VLSID conferences.*

1	**Code of the subject**	MTES-9202
2	**Title of the subject**	Nanoelectronics
3	**Any prerequisite**	Basic physics of Materials and Devices at Nanoscale
4	**L-T-P**	3-0-1
5	**Name of the proposer**	Anurag Srivastava
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	• This course will focus on developing better understanding the new perspective connecting the quantized conductance of short ballistic conductors to the familiar Ohm's law of long diffusive conductors, along with a brief description of the modern nanotransistor. • The major objectives are to provide students with knowledge and understanding of nano- electronics as an important interdisciplinary subject. • To have better understanding of electronics devices at quantum scale.
8	**Brief Contents (module wise)**	***Introduction:*** Device scaling, Impact of scaling and its limitations, Moore's law, role of quantum mechanics. ***Mesoscopic observables:*** Ballistic transport, phase interference, universal conductance fluctuations, weak localization; Carrier heating; ***Quantum Mechanics :*** Basic Quantum mechanics and Fermi statistics, Metals, Insulators and Semiconductor, Density of states (DOS) in 0D-3D, DOS in disordered materials, ***Physics of nanoelectronics devices***: concept of HOMO and LUMO, band gap etc. ;Two terminal device model: Current flow in the presence of a bias, numerical technique for self-consistent estimation of V-I ,Current flow, quantum of conductance, Landauer theory; Field Effect Transistors (FETs): Ballistic quantum wire FETs, conventional MOSFETs, CMOS, short channel and narrow width, hot electron effect, punch-through and thin gate oxide breakdown. ***Non-Classical Devices***: Single Electron Transistors, Resonant Tunneling Devices, Gate Around Silicon Nanowire Transistors, III-V Material Nanowire Transistors ***CNT, GNR, and Hybrid Materials –based Interconnects, Sensors and Energy Devices***
9	**Contents for lab (If applicable)**	Hands on tool Quantum ATK-VNL for electronic and transport properties of materials and devices.
10	**List of text books/references**	1. S. Datta, Electronic Transport in Mesocopic Systems; Cambridge University Press (1995). 2. S. Datta, Quantum Transport: Atom to Transistor; Cambridge University Press (2005). 3. David Ferry, Transport in Nanostructures Cambridge University Press (1995).

1	**Code of the subject**	MTES-9203
2	**Title of the subject**	Memory Design
3	**Any prerequisite**	NIL
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Gaurav Kaushal
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	The objective of the Memory Design is to acquaint the students with memory cell, memory peripherals, novel SRAM cell, next-generation memory and memory array. The subject gives the platform to analyze the read/write/hold operations of different memory structures using CAD tools.
8	**Brief Contents (module wise)**	Overview of volatile memory, non-volatile memory, on-chip memory, on-chip memory types. Review of CMOS circuit design, sensing circuitry basics, read/write assist circuitry and other peripheral circuitries, next generation SRAM cell. Introduction to DRAM, high speed DRAM architectures, open and folded arrays organizations, bandwidth, latency, and cycle time, power, timing circuits. STT-MRAM, data migration policy for hybrid cache. Operation of FLASH memories (FLASH array sensing and programming), Charge Pump circuits.
9	**Contents for lab (If applicable)**	No
10	**List of text books/references**	1) VLSI Memory Chip Design, by Kiyoo Itoh, Springer, 2001. 2) Ultra-low Voltage Nano-scale Memories, by Kiyoo Itoh, Masashi Horiguchi, Hitoshi Tanaka, Springer, 2009. 3) Semiconductor Memories: Technology, Testing, and Reliability, by Ashok K. Sharma, Wiley IEEE, 2013. 4) Semiconductor Memories: A Handbook of Design, Manufacture and Application, by Betty Prince, Wiley, 2nd Edison, 1996. 5) DRAM Circuit Design: Fundamental and High-Speed Topics, by Keeth, Baker, Johnson, and Lin, Wiley, IEEE 2007.

1	**Code of the subject**	MTES-9204
2	**Title of the subject**	Analog IC design
3	**Any prerequisite**	NA
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	At the end of the course the student will be able to: ➢ Understand the significance of different biasing styles and apply them aptly for different circuits. ➢ Design basic building blocks like sources, sinks, mirrors, up to layout level. ➢ Comprehend the stability issues of the systems and design Op-amp fully compensated against process, supply and temperature variations. ➢ Identify suitable topologies of the constituent sub systems and corresponding circuits as per the specifications of the system ➢ Design Analog integrated system including parasitic effects upto tape-out.
8	**Brief Contents**	**M I:** MOS FET device I/V characteristics, second order effects, Capacitances, body bias effect, Biasing Styles, MOS small signal Model, NMOS verses PMOS devices. **M II:** Basic building blocks and basic cells-Switches, active resistors, Current sources and sinks, Current mirrors: Basic current mirror, cascode current mirror, low voltage current mirror, Wilson and Widlar current mirrors, voltage and current references, Single stage amplifier: Common source stage with resistive load, diode connected load, triode load, CS stagewith source degeneration, source follower, CG stage, Gain boosting techniques, Cascode, folded cascode, choice of device models. **M III:** Differential amplifier: Quasi differential amplifier, significance of tail current source, errors due to mismatch, replication principle, qualitative analysis, common mode response, differential amplifier with MOS loads, single ended conversion, gilbert cell. Operational amplifier-characterization, 2 stage OP amp, process and temperature independent compensation, output stage.
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	1. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", McGraw-Hill, Inc., New York, USA. 2. Gabriel Alfonso Rincón-Mora, "Analog Ic Design - An Intuitive Approach", (Volume 2), lulu.com, 2014. 3. T. C. Carusone, D. Johns, K. Martin, "Analog Integrated Circuit Design, Wiley; 2nd edition, 2011. 4. P. R. Gray and R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", 5th Edition, Wiley, 2009. 5. Mohammed Ismail and Terri Fiez, "Analog VLSI: Signal and Information Processing", McGraw-Hill, 1994. 6. Geiger, Allen and Stradder, "VLSI Design Techniques for Analog and Digital Circuits", Tata McGraw-Hill Education, 2010.

1	**Code of the subject**	MTES-9205
2	**Title of the subject**	VLSI Architecture
3	**Any prerequisite**	Electronic Circuits and Digital Logic Design
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. SUNIL KUMAR
6	**Will this course require visiting faculty**	
7	**Learning Objectives of the subject (in about 50 words)**	The course objective is to cover the architecture design of VLSI systems and subsystems with the notion of optimization for area, speed, power dissipation, cost and reliability. Different aspects of VLSI system design and its applications in various field. The course also discusses traditional and state of the art analog and digital VLSI architectures optimized techniques.
8	**Brief Contents**	Module-I Overview of VLSI Design flow, Algorithm to architecture transformation - Graph based formalism and Isomorphic architecture. Pipelining and Parallel processing, Replication, and Time sharing. Module-II Architectural Synthesis and Optimization - synthesis problems, scheduling, sequencing graphs, hierarchical models, synchronization problem, data path and control unit synthesis. Module-III Clocking - single-phase and two-phase clocking, Asynchronous data processing architectures, Digital Signal Processing using array architectures- Systolic and wave-front arrays, wave-front arrays. Module-IV Analog array architectures- Architectural design of FPGA, scalability of FPAA. Algorithms for partitioning, floor- planning, placement, routing and compaction. Module-V Dynamically reconfigurable gate array -Static vs dynamic reconfiguration, single context vs multi-context dynamic reconfiguration, full vs partial run time reconfiguration.
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	1. Hubert Kaeslin, Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication, Cambridge University Press, 2009. 2. Giovanni De Micheli, Synthesis and Optimization of Digital Circuits, McGraw Hill, 2012 3. S.Y. Kung, "VLSI Array Processors", Prentice Hall, 2012 4. Magdy A. Bayoumi, VLSI Design Methodologies for Digital Signal Processing Architectures, Springer 2012.

1	**Code of the subject**	MTES-9206
2	**Title of the subject**	Hardware Security
3	**Any prerequisite**	Computer System Security, Integrated Circuit Technology, VLSI Design
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Saumya Bhadauria
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	• Learning the state-of-the-art security methods and devices • Better understanding of attacks and providing countermeasures against them
8	**Brief Contents (module wise)**	Module I: Fundamentals of hardware security and trust for integrated circuits. physical and invasive attacks, side-channel attacks and Countermeasures, physically unclonable functions, hardware-based true random number generators Module II: Watermarking of Intellectual Property (IP) blocks, FPGA security, passive and active metering for prevention of piracy, access control, hardware Trojan detection and isolation in IP cores and integrated circuits counterfeit ICs
9	**Contents for lab (If applicable)**	NIL
10	**List of text books/references**	• Mohammad Tehranipoor and Cliff Wang. 2011. *Introduction to Hardware Security and Trust*. Springer Publishing Company, Incorporated. • Debdeep Mukhopadhyay and Rajat Subhra Chakraborty, "Hardware Security: Design, Threats, and Safeguards", CRC Press • Ahmad-Reza Sadeghi and David Naccache (eds.): Towards Hardware-intrinsic Security: Theory and Practice, Springer.

1	**Code of the subject**	MTES-9207
2	**Title of the subject**	VLSI Physical Design Automation
3	**Any prerequisite**	NA
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Somesh Kumar
6	**Will this course require visiting faculty**	No
7	**Learning Objectives of the subject (in about 50 words)**	At the end of the course the student will be able to: ➢ Understand the relationship between design automation algorithms and various constraints posed by VLSI fabrication and design technology. ➢ Adapt the design algorithms to meet the critical design parameters. ➢ Identify layout optimization techniques and map them to the algorithms. ➢ Develop proto-type EDA tool and test its efficacy.
8	**Brief Contents**	**M I:** VLSI design Cycle, Physical Design Cycle, Design Rules, Layout of Basic Devices, and Additional Fabrication, Design styles: full custom, standard cell, gate arrays, field programmable gate arrays, sea of gates and comparison, system packaging styles, multichip modules. **M II:** Design rules, layout of basic devices, fabrication process and its impact on physical design, interconnect delay, noise and cross talk, yield and fabrication cost, Complexity Issues and NP-hard Problems, Basic Algorithms (Graph and Computational Geometry): graph search algorithms, spanning tree algorithms, shortest path algorithms, matching algorithms, min-cut and max-cut algorithms, Steiner tree algorithms **M III:** Basic Data Structures, atomic operations for layout editors, linked list of blocks, bin based methods, neighbor pointers, corner stitching, multi-layer operations, Graph algorithms for physical design: classes of graphs, graphs related to a set of lines, graphs related to set of rectangles, graph problems in physical design, maximum clique and minimum coloring, maximum k-independent set algorithm, algorithms for circle graphs **M IV:** Partitioning algorithms: design style specific partitioning problems, group migrated algorithms, simulated annealing and evolution, and Floor planning and pin assignment, Routing and placement algorithms
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	1. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, Kluwer Academic, 1999. 2. Charles J Alpert, Dinesh P Mehta, and Sachin S Sapatnekar, "Handbook of Algorithms for Physical Design Automation", CRC Press, 2008. 3. S. M. Sait, and H. Youssef, "VLSI Physical Design Automation", World Scientific. 4. S. Kyu, Lim, "Practical Problems in VLSI Physical Design Automation", Springer.

List of Electives for Semester III

1	**Code of the subject**	MTES-9301
2	**Title of the subject**	Energy Aware Computing
3	**Any prerequisite**	Basic VLSI design, basics of computer system organization
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Binod Prasad
6	**Will this course require visiting faculty**	Yes
7	**Learning Objectives of the subject (in about 50 words)**	➢ The course is intended to give an overview of the energy-dissipation aspects of computers and computing. To learn various power and energy consumption modeling and analysis. To make use of energy aware approach in different areas e.g., data center, storage system, and wireless networking .
8	**Brief Contents (module wise)**	**Module I:** Introduction, Power consumption basics, Regulations and industry initiatives- Government, Industry, Approaches for energy efficient computing- Product longevity, Algorithmic efficiency, Resource allocation, Gate/RT-level power modeling, Gate/RT-level power management, Micro-architecture power modeling, Micro-architecture-driven power management, Software power consumption, Compile-time power reduction techniques, Temporal and Spatial Data Mining Materials recycling, Tele-computing. **Module II:** Virtualization: Green Maturity model for Virtualization, Virtualization level, energy efficient storage: power efficient storage system, energy saving technique for disk storage, Thin Clients: Introduction and Characteristics, Dynamic Voltage/Frequency Scaling in microprocessor and small handheld gazettes. **Module III:** Middleware Support for green computing, Tools for monitoring, HPC computing, Green Mobile, embedded computing and networking, Management Frameworks Standards and metrics for green computing, power measuring and profiling: Profiling Energy Usages for the Application and the operating System, Extra Energy usages profile. **Module IV:** Green Networking: algorithmic aspects of energy aware computing, Taxonomy of Green Networking research: Adaptive Link rate, Interface Proxying, Energy aware Infrastructure, Energy ware Application, Efficient-Efficient Data Centers, energy efficient cellular Networking**:** Survey, energy performance metrics, energy Saving in Base Stations, Research Issues, Challenges, Wireless Sensor Network for Green Networking
9	**Contents for lab (If applicable)**	NA
10	**List of text books/references**	1. I. Ahmad, S. Ranka, "Handbook of Energy-Aware and Green Computing", CRC Press. 2. F. Richard Yu, Xi Zhang, Victor C.M. Leung, "Green Communications and Networking", CRC Press 3. B. Unhelkar, "Green IT Strategies and Applications: Using Environmental Intelligence", CRC Press, March 2011.

1	**Code of the subject**	MTES-9302
2	**Title of the subject**	Low Power VLSI Design
3	**Any prerequisite**	NO
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Pinku Ranjan
6	**Will this course require visiting faculty**	NO
7	**Learning Objectives of the subject (in about 50 words)**	➢ Identify clearly the sources of power consumption in a given VLSI Circuit ➢ Analyze and estimate dynamic and leakage power components in a DSM VLSI circuit ➢ Choose different types of SRAMs/ DRAMs for Low power applications ➢ Design low power arithmetic circuits and systems ➢ Decide at which level of abstraction it is advantageous to implement low power techniques in a VLSI system design
8	**Brief Contents (module wise)**	➢ Introduction, Sources Of Power Dissipation, Static Power Dissipation, Active Power ➢ Dissipation Designing for Low Power, Circuit Techniques For Leakage Power Reduction ➢ Standard Adder Cells, CMOS Adders Architectures, Low Voltage Low Power Design Techniques, Current Mode Adders ➢ Types Of Multiplier Architectures, Braun, Booth and Wallace Tree Multipliers and their performance comparison ➢ Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques ➢ The increased delays of wires, New materials for wires and dielectrics, Design methods taking into account interconnection delays, Cross talk ➢ Basic background on testing, Unsuitable design techniques for safety-critical applications, ➢ Low power and safely operating circuits, Case study – A Low power subsystem design
9	**Contents for lab (If applicable)**	NO
10	**List of text books/references**	1.Kiat Seng Yeo and Kaushik Roy, Low- Voltage, Low-Power VLSI Subsystems, Edition 2009, Tata Mc Graw Hill 2. Soudris D, Piguet C and Goutis C, Designing CMOS Circuits for Low Power, Kluwer Academic Publishers, 2002

1	**Code of the subject**	MTES-9303
2	**Title of the subject**	Spintronics Principles and Devices
3	**Any prerequisite**	Solid State Physics and Magnetic materials
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. SUNIL KUMAR
6	**Will this course require visiting faculty**	NO
7	**Learning Objectives of the subject (in about 50 words)**	The objective of this course is to cover a deeper insight in theories and practical knowledge of Spintronic Materials, Technology and Spin Devices for futuristic applications. It include introduction to spin and spin electronics, spin relaxation behavior, Spin dependent transport, Spin-transfer torque, Spin injections and spin devices, and Advances in spintronic materials, technology.
8	**Brief Contents (module wise)**	Module-I Overview of spin electronics, Types of magnetic ma- terials, Quantum Mechanics of spin, Spin-orbit interaction, Spin relaxation Module-II Spin dependent transport - Spin-dependent transport and tunneling. Andreev reflections, Point-Contact Andreev Reflection and their variants. Module-III spin transfer torque based MTJ, micromagnetics, Current-driven switching of magnetization; Current-Induced switch- ing in ferromagnetic wires and Domain wall scattering. Module-IV Spin injection, spin accumulation, and spin current, Spin hall effect, Spin LEDs, Electron spin filtering, Monolithic and Hybrid Spintronics. Module-V Materials for spin electronics, Nano-structures for spin electronics, Spin-Valve and spin-tunneling devices, Spintronic Biosensors, Quantum Computing with spins.
9	**Contents for lab (If applicable)**	NO
10	**List of text books/references**	1. S. Bandyopadhyay, M. Cahay, Introduction to Spintronics, CRC Press, 2008 2. D. J. Sellmyer, R. Skomski, Advanced Magnetic Nanostructures, Springer, 2006. 3. Y.B. Xu and S.M.Thompson, Spintronic Materials and Technol- ogy, Taylor and Francis, 2006. 4. M. Johnson, Magnetoelectronics, Academic Press 2004.

1	**Code of the subject**	MTES-9304
2	**Title of the subject**	System Level Design and Modelling
3	**Any prerequisite**	Digital Systems and Circuits, Programming in C/C++
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Dr. Santosh Singh Rathore
6	**Will this course require visiting faculty**	Yes
7	**Learning Objectives of the subject (in about 50 words)**	• To understand the concepts of multicore computing architectures ranging from low-power multiprocessor systems-on-chip (MpSoC) to high-performance chip-multiprocessors (CMP). • To understand fundamental topics on modeling, analysis and optimization of systems; and understand state-of-the-art methods, tools and techniques for system-level design and modelling.
8	**Brief Contents (module wise)**	**Module I:** Concurrency and embedded applications models, Network-on-chip communication, many-core architectures, cache hierarchy, performance analysis, scheduling, low-power and reliable design, dynamic power and thermal management, clocking. **Module II:** Use of hardware description languages (HDLs), FPGA prototyping, C++/SystemC and embedded multiprocessor platforms to implement complex applications. **Module III:** Embedded systems, electronic system-level (ESL) design, Models of Computation (MoCs): finite state machines (FSMs), dataflow, process networks, discrete event **Module IV:** System specification, profiling, analysis and estimation, System-level design: partitioning, scheduling, communication synthesis **Module V:** System-level modeling: processor and RTOS modeling, transaction-level modeling (TLM) for communication, System-level synthesis: design space exploration (DSE)
9	**Contents for lab (If applicable)**	None
10	**List of text books/references**	1. Umit Y. Ogras and Radu Marculescu. Modeling, Analysis and Optimization of Network-on-Chip Communication Architectures. Lecture Notes in Electrical Engineering, Vol. 184, Springer, 2013. 2. William Dally and Brian Towles. Principles and Practices of Interconnection Networks. Elsevier, 2004. 3. Jose Duato, Sudhakar Yalamanchili, and Lionel M. Ni. Interconnection Networks: An Engineering Approach. Morgan Kaufmann, 2003.

1	**Code of the subject**	MTES-9305
2	**Title of the subject**	Hardware Software Co-design
3	**Any prerequisite**	Computer Architectures, Computational Models
4	**L-T-P**	3-0-0
5	**Name of the proposer**	Debanjan Sadhya
6	**Will this course require visiting faculty**	Yes
7	**Learning Objectives of the subject (in about 50 words)**	• Analyze and explain the control-flow and data-flow of a software program and a cycle-based hardware description. • Transform simple software programs into cycle-based hardware descriptions with equivalent behaviour and vice versa. • Partition simple software programs into hardware and software components, and create appropriate hardware-software interfaces to reflect this partitioning. • Identify performance bottlenecks in a given hardware-software architecture and optimize them by transformations on hardware and software components.
8	**Brief Contents (module wise)**	**Module I**: Design of embedded systems: Characteristics of embedded applications The traditional design flow, What is bad with the traditional design flow, System-level design of embedded systems. **Module II**: Architectures and platforms for embedded systems: General purpose vs. application specific architectures, Typical architectures for embedded systems, Architecture specialization techniques, Component and platform-based Design, Reconfigurable Systems. **Module III**: Modeling techniques: Models of computations, Synchronous finite state machines, Time and synchrony, Globally asynchronous locally synchronous systems, Codesign finite state machines, System design with the POLIS system. **Module IV**: Performance analysis and co-simulation: Static analysis techniques, Worst case execution analysis, Micro-architectural modeling and analysis, Basic co-simulation approaches, Co-simulation of heterogeneous systems with Ptolemy. **Module V**: Optimization techniques for design space exploration: Optimization problems in codesign, Heuristic techniques, Simulated annealing, Tabu search, Genetic algorithms. **Module VI**: Software synthesis and code generation: Code selection techniques, Code selection and optimization for irregular architectures, Optimal storage assignment for DSP architectures, Retargetable compilers. **Module VII**: System-level power/energy optimization: Sources of power dissipation, System level power optimization, Dynamic power management, Mapping and scheduling for low energy, Real-time scheduling with dynamic voltage scaling.
9	**Contents for lab**	N/A
10	**List of text books/references**	1. "System-Level Synthesis", Ahmed A. Jerraya, Jean Mermet, *Kluwer Academic Publishers*. 2. "Hardware-Software Co-design of Embedded Systems. The POLIS Approach", Felice Balarin, *Kluwer Academic Publishers*.

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