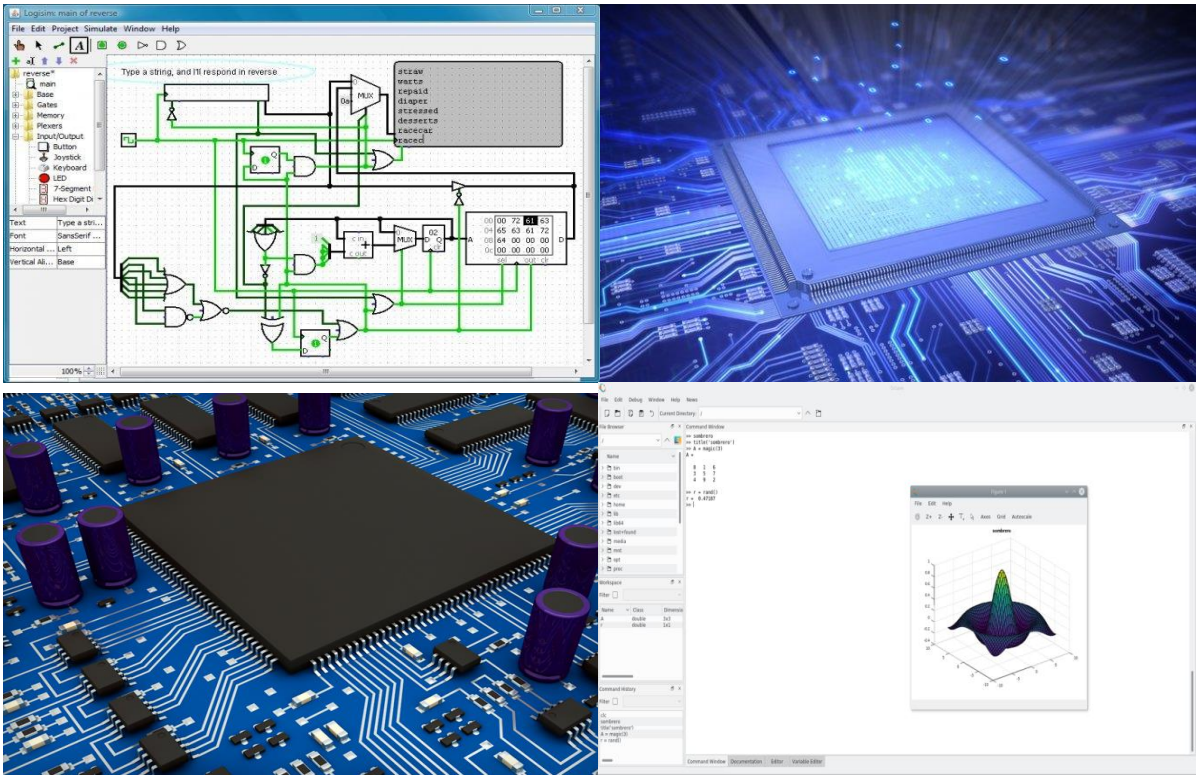
Curriculum & Contents

M. Tech.

(VLSI Design and Embedded Systems)



विश्वजीवनामृतं ज्ञानम्

ABV-Indian Institute of Information Technology & Management, Gwalior

June 2023

Name of the program -- M. Tech. (VLSI and Embedded Systems)

Total credit – 19+21+18+18 = 76

Credits for core courses	67
Credits for electives/MOOC courses	9

Semester I				
S. No.	**Subject Code**	**Title of the course**	**L-T-P**	**Credits**
1	EE-601	Digital IC Design	3-0-2	4
2	EE-602	System Design using HDL	3-0-2	4
3	EE-603	CAD for VLSI	3-0-2	4
4	EE-604	IC Technology	3-0-0	3
5	EE-605	Modelling and Simulation	3-0-2	4
			Total credits	**19**

Semester II				
S. No.	**Subject code**	**Title of the course**	**L-T-P**	**Credits**
1	EE-606	Analog IC Design	3-0-2	4
2	EE-607	Microcontroller and Embedded Systems	3-0-2	4
3		Elective-I	3-0-0	3
4		Elective-II	3-0-0	3
5		Art of Engineering Research	2-0-2	3
6		Machine Learning	3-0-2	4
			Total credits	**21**

Semester III				
S. No.	**Subject code**	**Title of the course**	**L-T-P**	**Credits**
1		Elective-III/MOOC course	3-0-0	3
2		Elective-IV/MOOC course	3-0-0	3
3	EE-698	Major Project part I	__	12
			Total credits	**18**

Semester IV				
S. No.	**Subject Code**	**Title of the course**	**L-T-P**	**Credits**
1		Elective-V/MOOC Course	3-0-0	3
2	EE-699	Major Project part II	__	15
			Total credits	**18**

List of Electives for VLSI Design and Embedded Systems

List of Electives for Semester II

S. No.	Subject Code	Course	L-T-P
1.	EE-051	Design Verification and Testing	3-0-0
2.	EE-052	VLSI Architecture	3-0-0
3.	EE-053	FPGA Based System Design	3-0-0
4.	EE-054	VLSI Signal Processing	3-0-0
5.	EE-055	Memory Devices and Circuits	3-0-0
6.	EE-056	Device and Interconnect Modelling	3-0-0

List of Electives for Semester III

S. No.	Subject Code	Course	L-T-P
1.	EE-057	Special Topics in VLSI and Embedded Systems	3-0-0
2.	EE-058	AI-Accelerator Design	3-0-0
3.	EE-059	Mixed Signal Design	3-0-0
4.	EE-060	RF Circuit Design	3-0-0
5.	EE-061	Hardware Security	3-0-0
6.	EE-062	Embedded Software	3-0-0
7.	EE-063	Network on Chip	3-0-0

List of Electives for Semester IV

S. No.	Subject Code	Course	L-T-P
1.	EE-064	Low Power VLSI	3-0-0
2.	EE-065	Quantum electronics	3-0-0
3.	EE-066	Sensors for autonomous system	3-0-0
4.	EE-067	High Performance Computing Systems	3-0-0

1	**Semester**	I
2	**Type of course**	Core
3	**Code of the subject**	EE-601
4	**Title of the subject**	Digital IC Design
5	**Any prerequisite**	NIL
6	**L-T-P**	3-0-2
7	**Learning Objectives of the subject**	This course aims to convey knowledge of basic concepts of digital VLSI circuit design using CMOS and state-of-the-art device technologies with an emphasis on "hands-on" IC design using ECAD/CAD tools. Emphasis is on the circuit design, optimization, and layout of very high speed, high density or low power circuits for use in applications such as processors, signal and memory and periphery. Special attention will be devoted to the most important challenges facing digital circuit designers today and in the coming decade, being the impact of scaling, deep submicron effects, interconnect, signal integrity, power distribution and consumption for energy efficient and PVT aware real-time applications. Students should be able to apply their knowledge of electronics and engineering in the design of CMOS integrated circuits and digital VLSI design as per the need of current academia and VLSI industry. This will be reflected in both the lecture and laboratory classes.
8	**Brief Contents**	Introduction and future prospects, Evolution of CMOS transistor structure, Modeling of transistor using SPICE, Inverters static characteristics, Inverters switching characteristics and interconnect effects; Combinational logic circuits, Sequential logic circuits, Dynamic logic circuits, Semiconductor memories, Low power logic circuits, High-speed circuits

1	**Semester**	I
2	**Type of course**	Core
3	**Code of the subject**	EE-602
4	**Title of the subject**	System Design using HDL
5	**Any prerequisite**	Digital Electronics in UG
6	**L-T-P**	3-0-2
7	**Learning Objectives of the subject (in about 50 words)**	Correctly describe the detailed behaviour of given digital logic circuits as defined by Verilog HDL, state diagrams, or other means, including those circuits related to modern computer architecture. Translate system requirements into a practical digital design, making use of modern engineering tools such as Xilinx Vivado, Verilog HDL, and FPGA prototyping boards. Model the digital designs including FSMs to Processor architectures using the knowledge of HDL Language Apply the knowledge of Reconfigurable architectures like FPGAs in designing and implementing digital ICs.
8	**Brief Contents**	Basic concepts of hardware description languages (VHDL, Verilog HDL), Logic and delay modeling, Structural, Data-flow and Behavioral styles of hardware description, Architecture of event driven simulators, Operators, Operands, Operator types, Blocking and non-blocking statements, Delay control, Generate statement, Event control, Sequential Logic Design, FSM, Configuration Specifications, Sub-Programs, Test Benches. Types of Reconfiguration, Details study of FPGA, Design tradeoffs, Bidirectional wires and switches, FPGA Placement: Placement Algorithms, FPGA Routing, Timing Analysis, Network Virtualization with FPGAs, On-chip Monitoring Infrastructures, Multi-FPGA System Software, Logic Emulation, Applications, High Level Compilation

1	**Semester**	I
2	**Type of course**	Core
3	**Code of the subject**	EE-603
4	**Title of the subject**	CAD for VLSI
5	**Any prerequisite**	Digital Design, Data Structures and Algorithms
6	**L-T-P**	3-0-2
7	**Learning Objectives of the subject (in about 50 words)**	The main objective of this course is to provide in-depth understanding of the theoretical as well as practical concepts of the designing algorithms for CAD tools for VLSI design. The students will be able to identify and develop new algorithms and CAD tools for VLSI design. The scope of this course is also to visualize new Design Automation (DA) research problems in view of the challenges of designing multi-core and/or many-core system-on-chip in the nanometer regime. Another objective of this course is to give the exposure to machine learning and deep learning algorithms for designing efficient hardware in IOT era.
8	**Brief Contents (module wise)**	Introduction to VLSI-CAD, module generation, PLAs and FPGAs, Digital hardware modeling, benchmark circuits (ISCAS'85, ISCAS'89…), Simulation algorithms design verification, graph data structure and algorithms for VLSI-CAD, High-level synthesis, Algorithms for physical design automation, slicing and non-slicing floorplans, polar graphs and adjacency graphs for floorplans, Introducing NOC as a future SOC paradigm, Timing analysis, SDC, set-up & hold time concept, timing exceptions, set-up & hold calculations, noise analysis.

1	**Semester**	I
2	**Type of course**	Core
3	**Code of the subject**	EE-604
4	**Title of the subject**	IC Technology
5	**Any prerequisite**	Nil
6	**L.T.P.**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	Students will be able to learn flow of IC Design which includes fundamental of fabrication to chip, input output packaging, interconnection network. To demonstrate a clear understanding of CMOS fabrication flow, input/output circuits, chip packaging Get the idea of data flow in interconnection network, routing and topology basics.
8	**Brief Contents**	Design flow using, ASIC, SoC, FPGA, Full custom, Semicustom CMOS Technology, GaAs Technology, Bipolar-CMOS-DMOS (BCD) Technology, Advanced Process Technology CMOS Process flow, IC Manufacturing, Input Output Interfacing, Input Circuits, Output circuits, ESD, Packaging, Signal Integrity Electrical Testing, Yield, Future trends, and Challenges: Challenges for integration, system on chip, Novel Devices.

1	**Semester**	I
2	**Type of course**	Core
3	**Code of the subject**	EE-605
4	**Title of the subject**	Modelling and Simulation
5	**Any prerequisite**	VLSI Design, Electronics Devices and Circuits
6	**L-T-P**	3-0-2
7	**Learning Objectivesof the subject (in about 50 words)**	The objective of the course is to provide the fundamental knowledge for understanding concepts of semiconductor devices. Upon successful completion of the course, students will be able to graspfundamental knowledge of semiconductor devices for Integrated Circuit design. Be able to model the devices using SPICE modeling.
8	**Brief Contents**	Device Level Modeling: PN Junction, MOSFET, Limitation of long channel analysis, Short-channel effects, Technology nodes and ITRS, Physical & technological challenges to scaling, nonconventional MOSFET (FDSOI, SOI, Multi-gate MOSFETs), Verilog-A model Interconnect Modelling: Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parameters Circuit Modelling: Circuit simulation using available device model, Netlist, System Modelling: System Bus protocols (AMBA AXI, AHB, APB), AXI/AHB hub/interconnect for multi-master multi-slave design, Synthesis, FPGA implementation, Pin mapping, Bitstream generation, Exporting design to SDK.

1	**Semester**	II
2	**Type of course**	Core
3	**Code of the subject**	EE-606
4	**Title of the subject**	Analog IC Design
5	**Any prerequisite**	Digital IC Design ( )
6	**L-T-P**	3-0-2
7	**Learning Objectives of the subject (in about 50 words)**	On completion of this course, the students will be able to: acquire a basic knowledge of analog IC design including small signal models, and analog MOS processes. design of single stage and differential stage amplifiers with and without current mirror circuits, respectively. analyze the frequency responses of single-stage amplifiers. analyze and design two-stage operational amplifier. identify the different types of noises in analog integrated circuits.
8	**Brief Contents**	Small signal Models, Amplifiers and Current sources: Large Signal and Small-Signal analysis of common source stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode, Differential amplifier, current Sources, Basic Current Mirrors, Cascode Current Mirrors and current mirror based differential amplifier, Frequency Response of Amplifiers, Feedback, Operational Amplifier, Noise, Determination of dominants poles; Compensation and relocation of poles and zeros

1	**Semester**	II
2	**Type of course**	Core
3	**Code of the subject**	EE-607
4	**Title of the subject**	Microcontroller and Embedded System
5	**Any prerequisite**	Nil
6	**L-T-P**	3-0-2
7	**Learning Objectives of the subject (in about 50 words)**	The student will be able to: Understand the concept of embedded system, microcontroller, different components of microcontroller and their interactions. Get familiarized with programming environment to develop embedded solutions. Program ARM microcontroller to perform various tasks. Understand the key concepts of embedded systems such as I/O, timers, interrupts and interaction with peripheral devices.
8	**Brief Contents**	8051 Microcontroller, PIC Microcontrollers, RM7TDMI Microcontrollers, Hardware Interfacing: Interfacing with LEDs, Seven Segment, Sensors, Basic concepts of LCD, ADC, DAC, Relays etc. and their interfacing to microcontroller. Introduction to Embedded Systems: Background, History and classification, Core of the embedded system-general purpose and domain-specific processors, ASICs, PLDs, COTs; Communication Interface, Embedded Firmware Design and Development, RTOS Based Embedded System Design.

1	**Semester**	II
2	**Type of course**	Core
3	**Code of the subject**	
4	**Title of the subject**	Art of Engineering Research
5	**Any prerequisite**	NIL
6	**L-T-P**	2-0-2
7	**Learning Objectives of the subject (in about 50 words)**	To enable a student to develop their theoretical, methodological and research skills to enhance their ability to conduct rigorous research and reach to sound evidence-based conclusions. Understanding the nature of problem to be studied and identifying the related area of knowledge. Reviewing literature to understand how others have approached or dealt with the problem. Collecting data in an organized and controlled manner so as to arrive at valid decisions. Analyzing data appropriate to the problem. The motive behind data analysis in research is to present accurate and reliable data. As far as possible, avoid statistical errors, and find a way to deal with everyday challenges like outliers, missing data, data altering, data mining, or developing graphical representation.
8	**Brief Contents**	Introduction to research - Research Methods in Engineering, Research paper analysis, Data analysis of reported data, Advance trends in electrical and electronics engineering, Review Process, Review guidelines, Validity threats, Review decisions, Qualitative Methods, Study Designs, Elements, and Methods, The nature and types of qualitative research, Data collection methods - primary and secondary sources, Types of data analysis methods, Survey Research, Sampling Methods, Survey Study Designs, Case Studies. Introduction to Mixed Methods Research, Study Designs and Method, Writing research papers, purpose, nature and evaluation, content and format, Research Presentations, The Art of Scientific and Technical Writing.
9	**Contents for lab (If applicable)**	1. Problem statement Practice 2. Literature Survey Practice 3. Technical Paper writing – Practice 4. Presentation - Practice

1	**Semester**	II
2	**Type of course**	Core
3	**Code of the subject**	
4	**Title of the subject**	Machine Learning
5	**Any prerequisite**	NIL
6	**L-T-P**	3-0-2
7	**Learning Objectives of the subject (in about 50 words)**	To understand popular ML algorithms with their associated mathematical foundations for appreciating these algorithms, To help connect real-world problems to appropriate ML algorithm(s) for solving them and to enable formulating real world problems as machine learning tasks
8	**Brief Contents**	Introduction to ML, Fundamentals of ML - PCA and Dimensionality Reduction,Nearest Neighbours and KNN, Linear Regression, Decision Tree Classifiers. Notion of Generalization and concern of Overfitting, Notion of Training, Validation and Testing; Connect to generalisation and overfitting. Selected Algorithms - Ensembling and RF, Linear SVM, K Means,Logistic Regression, Naive Bayes, Neural Network Learning - Role of Loss Functions and Optimization, Gradient Descent and Perceptron/Delta Learning, MLP, Backpropagation, MLP for Classification and Regression, Regularisation, Early Stopping, Kernels (with SVM), Bayesian Methods, Generative Methods, HMM, EM, PAC learning, Introduction to Deep Learning, CNNs, Popular CNN Architectures, RNNs, GANS and Generative Models, Advances in Backpropagation and Optimization for Neural Networks Adversarial Learning
9	**Contents for lab (If applicable)**	To implement basic algorithms using basic machine learning libraries mostly in python. Gain hands-on experience in applying ML to problems encountered in various domains. In addition, obtain exposure to high-level ML libraries or frameworks such as TensorFlow, PyTorch.

1	**Semester**	II
2	**Type of course**	Elective
3	**Code of the subject**	EE-051
4	**Title of the subject**	Design Verification and Testing
5	**Any prerequisite**	CAD for VLSI
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	The main objective of this course is to provide in-depth understanding of the problems encountered in testing large circuits, approaches to detect and diagnose the faults and methods to improve the design to make it testable. The students will be able to develop algorithms and tools for VLSI testing, designing of testable and trustworthy circuits. The scope of this course is to particularly address the challenges in the VLSI testing domain and get motivated towards research in this field.
8	**Brief Contents (module wise)**	Introduction and Fault Modeling, Testing Techniques, Time frame expansion methods, Boolean Satisfiability, Transitive-closure based and Neural Network based approaches, Fault Simulation, Design for Testability and Built-in-self-test, Controllability and observability measures, TEMEAS, SCOAP, Ad-hoc design built-in-logic-block-observer (BILBO), Linear feedback shift register (LFSR), Theory of LFSRs, Design for Trust Techniques: Different Types of Attacks, Counter Measures for different types of attacks, Prevention based Approaches, Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages, Introduction to Hardware Verification methodologies, Verifications based on simulation, Analytical and formal approaches. Functional verification, Timing verification, Formal verification. Basics of equivalence checking and model checking
9	**Contents for lab (If applicable)**	NA

1	**Semester**	II
2	**Type of course**	Elective
3	**Code of the subject**	EE-052
4	**Title of the subject**	VLSI Architecture
5	**Any prerequisite**	System Design using HDL
6	**L-T-P**	3-0-0
7	**Learning Objectivesof the subject (in about 50 words)**	The course objective is to cover the architecture design of VLSI systems and subsystems with the notion of optimization for area, speed, power dissipation, cost and reliability. Different aspects of VLSI system design and its applications invarious field. The course also discusses traditional and state of the art analog and digital VLSI architectures optimized techniques.
8	**Brief Contents**	ISA, Datapath and control path design, Single Cycle MIPS , 5 Stage pipeline MIPS, CISC Architecture, RISC architecture, Arithmetic unit design, Fixed point and floating point, memory units, Optimization, Instruction level parallelism, Super scalar processor, Multi-core and multi thread Architecture, Network on chip, Dynamically reconfigurable gate array, Static vs dynamic reconfiguration, Single context vs multi-context dynamic reconfiguration, Full vs partial run time reconfiguration.
9	**Contents for lab (Ifapplicable)**	NA

1	**Semester**	II
2	**Type of course**	Elective
3	**Code of the subject**	EE-053
4	**Title of the subject**	FPGA Based System Design
5	**Any prerequisite**	Nil
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	The goal of the course is to study the basic principles and methods of FPGA prototyping. Understanding of principles of IC prototyping; hardware and software; design strategies and methods
8	**Brief Contents (module wise)**	ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques. Architecture of ROM – ROM Programming – Architecture of SPLDs – SPLDs programming – Architecture of CPLDs – Basics of FPGAs– Structure of FPGAs Implementation of Digital circuits in FPGA processor, Education FPGA kit – FPGA pin assignment – Interfacing Input/Output devices with FPGA, SPI, I2C, I3C, UART protocol RTL design System Design Examples using Xillinx FPGAs – Traffic light Controller, Real Time Clock, VGA, Keyboard, LCD, Embedded Processor Hardware Design
9	**Contents for lab (If applicable)**	No

1	**Semester**	II
2	**Type of course**	Elective
3	**Code of the subject**	EE-054
4	**Title of the subject**	VLSI Signal Processing
5	**Any prerequisite**	Digital Circuit, and Signals & Systems
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	This course aims at providing comprehensive coverage of the important techniques for designing efficient VLSI architectures for DSP. This course will enable students to understand industrial challenges in the implementation of DSP systems, like capability to process high throughput data in real-time, as well as requiring less power and less chip area.
8	**Brief Contents (module wise)**	Graphical representation of DSP algorithms, Signal flow graph (SFG), Data flow graph (DFG) and dependence graph (DG), High-level transformation, Critical path, Retiming of DFG, Critical path minimization by retiming, Loop retiming and iteration bound, Cutset retiming, Design of pipelined DSP architectures. Parallel realization of DSP algorithms, Unfolding theorem, Polyphase decomposition, Hardware efficient parallel realization of FIR filters, 2-parallel and 3-parallel filter architectures, Hardware minimization by folding, Delay optimization by folding, Lifetime analysis. Pipelining digital filters, Combining parallel processing with pipelining in digital filters.
9	**Contents for lab (If applicable)**	NA

1	**Semester**	II
2	**Type of course**	Elective
3	**Code of the subject**	EE-055
4	**Title of the subject**	Memory Devices and Circuits
5	**Any prerequisite**	Digital IC Design
6	**L-T-P**	3-0-0
7	**Learning Objectivesof the subject (in about 50 words)**	The objective of the Memory Design is to acquaint the students with memory cell, memory peripherals, novel SRAM cell, next-generation memory. The subject gives the platform to analyze the read/write/hold operations of different memory structures using CAD tools.
8	**Brief Contents (module wise)**	Overview of volatile memory, Non-volatile memory, On-chip memory, On-chip memory types. Review of CMOS circuit design, Sensing circuitry basics, Read/write assist circuitry and other peripheral circuitries, Next generation SRAM cell. Introduction to DRAM, High speed DRAM architectures, Open and folded arrays organizations, Bandwidth, latency, and Cycle time, Power, Timing circuits. STT-MRAM, Data migration policy for hybrid cache. Operation of FLASH memories (FLASH array sensing and programming), Charge Pump circuits. Basic of memory compiler for SRAM architecture using scripting language
9	**Contents for lab (Ifapplicable)**	NA

1	**Semester**	II
2	**Type of course**	Elective
3	**Code of the subject**	EE-056
4	**Title of the subject**	Device and Interconnect Modelling
5	**Any prerequisite**	NIL
6	**L-T-P**	3-0-0
7	**Learning Objectivesof the subject (in about 50 words)**	Upon the completion of this course, the students are able to: Concept of MOS modeling Understand the advanced interconnect materials. Acquire knowledge about Technology trends, Device and interconnect scaling. Identify basic device and Interconnect Models. Perform RLC based Interconnect analysis. Analyse the problem with existing material in deep submicron.
8	**Brief Contents**	Technology trends, Device and interconnect scaling, Interconnect Models: RC model and RLC model, Effect of capacitive coupling, Effect of inductive coupling, Transmission line model, Power dissipation, Interconnect reliability, Driver and Load Device Models, Interconnect Analysis, Time domain analysis, RLC network analysis, RC network analysis and responses in time domain, S domain analysis, Circuit reduction via matrix approximation, Analysis using moment matching, Crosstalk Analysis, Advanced Interconnect Materials. Introduction to the TCAD Simulation Tool, Examples of TCAD Simulations, Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, Two terminal MOS Device threshold voltage modelling, C-V Characteristics, Four terminal MOSFET threshold voltage I-V modelling, Short channel effect (SCE), High-K gate dielectric, Nonconventional MOSFET – (FDSOI, SOI, Multi-gate MOSFETs). Nonconventional MOSFET – (FDSOI, SOI, Multi-gate MOSFETs).
9	**Contents for lab (Ifapplicable)**	Circuit simulation using compact model, Verilog-A model. Vivado HLS flows to model system design, c/c++ coding for Vivado SDK

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-057
4	**Title of the subject**	Special Topics in VLSI and Embedded Systems
5	**Any prerequisite**	NIL
6	**L-T-P**	3-0-0
7	**Learning Objectivesof the subject (in about 50 words)**	This will focus on special topics of contemporary relevance and interest to both industry and research.
8	**Contents for lab (Ifapplicable)**	NA

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-058
4	**Title of the subject**	AI-Accelerator Design
5	**Any prerequisite**	NIL
6	**L-T-P**	3-0-0
7	**Learning Objectivesof the subject (in about 50 words)**	This course provides in-depth coverage of the architectural techniques used to design accelerators for training and inference in machine learning systems. Get exposure of implementation of CNN network in FPGA board. Get an idea about data system bus used in communication between different system blocks. To design energy-efficient accelerators, develop the intuition to make trade-offs between ML model parameters and hardware implementation techniques.
8	**Brief Contents**	Deep understanding of Neural networks, Linear algebra fundamentals and accelerating linear algebra, Implementation of Deep Learning Kernels, Zynq series FPGA architecture, interface knowledge, high speed protocol (Ethernet 100/10 Gbps), c/c++ coding for Vivado SDK, activation function verilog implementation, classification layer HDL implementation, SPI, I2C, I3C, UART protocol RTL design.
9	**Contents for lab (Ifapplicable)**	NA

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-059
4	**Title of the subject**	Mixed Signal Design
5	**Any prerequisite**	Analog IC Design
6	**L-T-P**	3-0-0
7	**Learning Objectivesof the subject (in about 50 words)**	At the end of the course the student will be able to: Understand the significance of different biasing styles and apply them aptly fordifferent circuits. Design basic building blocks like sources, sinks, mirrors, up to layout level. Comprehend the stability issues of the systems and design Op-amp fully compensated against process, supply and temperature variations. Identify suitable topologies of the constituent sub systems and correspondingcircuits as per the specifications of the system Design Analog integrated system including parasitic effects upto tape-out.
8	**Brief Contents**	Process and temperature independent compensation, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit. Performance of Sample-and-Hold Circuits, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Jitter and Phase Noise, Period Jitter, Probability Density Function of Jitter, Ring Oscillators, LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLS
9	**Contents for lab (Ifapplicable)**	NA

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-060
4	**Title of the subject**	RF Circuit Design
5	**Any prerequisite**	Analog IC Design
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	Get the idea of various parameters of interest in RF systems. To understand issues involved in design for GHz frequencies. To understand theoretical background relevant for design of active and passive circuits for RF front end in wireless digital communication systems.
8	**Brief Contents (module wise)**	Characteristics of passive components for RF circuits. Passive RLC networks. Transmission lines. Two-port network modeling. S-parameter model. The Smith Chart and its applications, Active devices for RF circuits: SiGe MOSFET, GaAs pHEMT, HBT and MESFET. RF Amplifier design: single and multi-stage amplifiers. Review of analog filter design. Voltage references and biasing. Low Noise Amplifier design: noise types and their characterization, LNA topologies, Power match vs Noise match. Linearity and large-signal performance, RF Power amplifiers: General properties. Class A, AB and C Power amplifiers. Class D, E and F amplifiers. Modulation of power amplifiers, Analog communication circuits, Phase-locked loops, Oscillators and synthesizers.
9	**Contents for lab (If applicable)**	No

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-061
4	**Title of the subject**	Hardware Security
5	**Any prerequisite**	VLSI Design
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (inabout 50 words)**	Learning the state-of-the-art security methods and devices Better understanding of attacks and providing countermeasures against them
8	**Brief Contents (module wise)**	Module I: Fundamentals of hardware security and trust for integrated circuits. Physical and invasive attacks, Side-channel attacks and Countermeasures, Physically unclonable functions, Hardware-based true random number generators Module II: Watermarking of Intellectual Property (IP) blocks, FPGA security, Passive and active metering for prevention of piracy, Access control, Hardware Trojan detection and isolation in IP cores and integrated circuits counterfeit ICs
9	**Contents for lab (Ifapplicable)**	NA

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-062
4	**Title of the subject**	Embedded Software
5	**Any prerequisite**	Nil
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	Analyze and explain the control-flow and data-flow of a software program and acycle-based hardware description. Transform simple software programs into cycle-based hardware descriptionswith equivalent behavior and vice versa. Partition simple software programs into hardware and software components, andcreate appropriate hardware-software interfaces to reflect this partitioning. Identify performance bottlenecks in a given hardware-software architecture andoptimize them by transformations on hardware and software components.
8	**Brief Contents (module wise)**	Design of embedded systems, Architectures and platforms for embedded systems, General purpose vs. application specific architectures, Reconfigurable Systems, Modeling techniques, Models of computations, Synchronous finite statemachines, Time and synchrony, Co-design finite state machines, System design with the POLIS system, Performance analysis and co-simulation, Static analysis techniques,Co-simulation of heterogeneous systems with Ptolemy, Optimization techniques for design space exploration, Software synthesis and code generation, Retargetable compilers, System-level power/energy optimization Mapping and scheduling for low energy, Real-time scheduling with dynamic voltage scaling.
9	**Contents for lab**	NA

1	**Semester**	III
2	**Type of course**	Elective
3	**Code of the subject**	EE-063
4	**Title of the subject**	Network on Chip
5	**Any prerequisite**	NIL
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	Upon completion of this course, students will be able to: Compare different architecture design. Understand the different routing algorithms. Understand the three dimensional networks-on-chip architectures Analyze test and fault tolerance of Communications in NOC Apply the 3D Integration procedures in NOC
8	**Brief Contents (module wise)**	Introduction to NoC, OSI layer rules in NoC, Interconnection Networks in Network-on-Chip Network Topologies, Switching Techniques, Routing Strategies, Architecture Design, Switching Techniques and Packet Format, Asynchronous FIFO Design, Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design, Routing Algorithms, Test and Fault Tolerance of NOC, 3-D integration of NOC
9	**Contents for lab (If applicable)**	NA

1	**Semester**	IV
2	**Type of course**	Elective
3	**Code of the subject**	EE-064
4	**Title of the subject**	Low Power VLSI
5	**Any prerequisite**	Digital IC Design
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	Correctly describe the detailed behaviour of given digital logic circuits as defined by Verilog HDL, state diagrams, or other means, including those circuits related to modern computer architecture. Translate system requirements into a practical digital design, making use of modern engineering tools such as Xilinx Vivado, Verilog HDL, and FPGA prototyping boards. Demonstrate the ability to modify existing HDL code to meet new system requirements. Demonstrate hands-on test bench and prototyping skills to ensure that a design meets the specified system requirements.
8	**Brief Contents**	Introduction: Need for low-power VLSI chips, Sources of power dissipation on Digital Integrated circuits, Dynamic dissipation, Static Dissipation, Technology & Device innovation, Emerging Low power approaches, Low power design techniques at architecture and system levels, Power consumption of dedicated hardware vs. software implementations of systems, Low power architecture, RTL design techniques for low power, UPF, Low power random access memory circuits, Power analysis and design at system level
9	**Contents for lab (If applicable)**	NA

1	**Semester**	IV
2	**Type of course**	Elective
3	**Code of the subject**	EE-065
4	**Title of the subject**	High Performance Computing Systems
5	**Any prerequisite**	VLSI Architecture
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	To get in-depth analysis of issues in High Performance Computing systems including: (1) Parallel Computing (2) New Processor Architectures, (3) Power-Aware Computing and Communication, (4) Advanced Topics on Petascale Computing and Optical Systems. To understand parallel models of computation such as dataflow, and demand-driven computation.
8	**Brief Contents (module wise)**	Parallel Processing Concepts; Levels and model of parallelism: Instruction, Transaction, Task, Thread, Memory, Function, Data Flow models, Demand-driven computation; Parallel architectures: Superscalar architectures, Multi-core, Multi-threaded, Server and cloud; Fundamental design issues in HPC: Load balancing, scheduling, Synchronization and resource management; Operating systems for scalable HPC; Parallel languages and programming environments; Fundamental limitations in HPC, Benchmarking HPC, Scalable storage systems, Accelerated HPC, Power-aware HPC Design.
9	**Contents for lab (If applicable)**	No

1	**Semester**	IV
2	**Type of course**	Elective
3	**Code of the subject**	EE-066
4	**Title of the subject**	Sensors for Autonomous System
5	**Any prerequisite**	Nil
6	**L-T-P**	3-0-0
7	**Name of the Faculty**	
8	**Will this course require visiting faculty**	No
9	**Learning Objectives of the subject (in about 50 words)**	Acquire knowledge about Micro Sensors. Get the idea about sensor application for autonomous system
10	**Brief Contents**	Introduction and historical background, Microsensors : Sensors and characteristics, Integrated Smart sensors, Sensor Principles/classification- Physical sensors (Thermal sensors, Electrical Sensors, Tactile sensors, accelerometers, gyroscopes , Proximity sensors, Angular displacement sensors, Rotational measurement sensors, Pressure sensors, Flow sensors, MEMS microphones etc.), Chemical and Biological sensors (chemical sensors, Molecule-based biosensors, Cell-based biosensors), Transduction methods (Optical, Electrostatic, Electromagnetic, Capacitive, Piezoelectric, Piezoresistive etc.), Application for Autonomous System
11	**Contents for lab (If applicable)**	NA

1	**Semester**	IV
2	**Type of course**	Elective
3	**Code of the subject**	EE-067
4	**Title of the subject**	Quantum electronics
5	**Any prerequisite**	Digital IC Design
6	**L-T-P**	3-0-0
7	**Learning Objectives of the subject (in about 50 words)**	The course gives an introduction to solid state physics, and will enable the student to employ classical and quantum mechanical theories needed to understand the physical properties of solids. Emphasis is put on building models able to explain several different phenomena in the solid state.
8	**Brief Contents**	The crystal structure of solids, Introduction to quantum mechanics: Principles of Quantum mechanics, Application of Schrodinger's Wave Equations, Introduction to Quantum Theory of Solids: The kronig-Penney Model, Electrical conduction in Solids, DOS, Statistical Mechanics, The semiconductor in Equilibrium Carrier transport Phenomenon, Non-equilibrium Excess Carriers in Semiconductor, PN-Junction, MOSCAP, Thin film Transistors, QCA
9	**Contents for lab (If applicable)**	NA